CLAIMS

1. A method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region, the method comprising:

forming recess gate holes in the substrate within the cell region;

forming a gate oxide layer in the recessed gate holes and in the peripheral region;

forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and

simultaneously patterning the gate layer and the gate oxide layer to form recessed cell gate structures in the cell region and planar cell gate structures in the peripheral region.

2. The method of claim 1, further comprising:

simultaneously forming spacer structures on the cell gate structures in the cell region and the planar cell gate structures in the peripheral region.

3. The method of claim 1, further comprising, prior to forming the recess gate holes:

sequentially forming a pad oxide layer, an etch stop layer, and a protective oxide layer in both the cell region and the periphery region of the substrate.

4. The method of claim 3, further comprising:

etching the protective oxide layer, the etch stop layer, and the pad oxide layer.

5. The method of claim 4, further comprising:

forming spacer structures on the cell gate structures in the cell region and the planar cell gate structures in the peripheral region; and

wherein etching the layers occurs after forming the spacer structures.

6. The method of claim 1, further comprising forming a Cosi layer in the peripheral region of the substrate.

7. A method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region, the method comprising:

forming recess gate holes in the substrate within the cell region and the periphery region;

forming a gate oxide layer in the recessed gate holes;

forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and

simultaneously patterning the gate layer and the gate oxide layer to form recessed cell gate structures in the cell region and in the periphery region.

8. The method of claim 7, further comprising:

simultaneously forming spacer structures on the cell gate structures in the cell region and in the peripheral region.

9. The method of claim 7, further comprising, prior to forming the recess gate holes:

sequentially forming a pad oxide layer, an etch stop layer, and a protective oxide layer in both the cell region and the periphery region of the substrate.

10. The method of claim 9, further comprising:

etching the protective oxide layer, the etch stop layer, and the pad oxide layer.

11. The method of claim 10, further comprising:

forming spacer structures on the cell gate structures in the cell region and in the peripheral region; and

wherein etching the layers occurs after forming the spacer structures.

12. A method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region, the method comprising:

forming a disposable layer disposed on the semiconductor substrate;

forming a first set of gate patterns in the disposable layer over the cell region;

forming a gate forming hole in the disposable layer over the periphery region;

forming recess gate holes in the substrate within the cell region through the first set of gate patterns;

forming a gate oxide layer in the recessed gate holes and in the gate forming hole;

forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and

removing the disposable layer to form recessed cell gate structures in the cell region and cell gate structures in the peripheral region.

13. The method of claim 12, further comprising:

simultaneously forming spacer structures on the cell gate structures in the cell region and the cell gate structures in the peripheral region.

14. A memory device, comprising:

a substrate divided into a memory cell region and a peripheral circuit region;

a plurality of memory cells having recessed gates formed in the memory cell region; and

at least one transistor in the peripheral circuit region, the transistor including:

a channel region formed between a source region and a drain region,

a gate structure disposed over the channel region, and

a resistance-reducing layer formed over the source and drain regions.

15. The memory device of claim 14 wherein the resistance-reducing layer comprises Cobalt.

16. The memory device of claim 15 wherein the resistance-reducing layer comprises a Cobalt-Silicon material.

17. The memory device of claim 14, further comprising an epitaxially grown silicon structure disposed between the source and drain regions and the resistance-reducing layer.

18. The memory device of claim 17 wherein the epitaxially grown silicon structure is formed by SEG (Selective Epitaxial Growing).

20. A method for forming a memory device on a substrate having a memory cell region and a peripheral region, the method comprising:

growing isolation structures to define a plurality of memory cells in the memory cell region, and to define a plurality of transistors in the peripheral region;

forming a pad oxide layer on the substrate in both the memory cell region and the peripheral region;

forming an etch stopping layer on the pad oxide layer;

forming a protective oxide layer on the pad oxide layer;

depositing a photoresist layer over the protective oxide layer;

forming a recess mask in the photoresist layer in the memory cell region;

etching the substrate in the memory cell region through the recess mask to form a plurality of recessed gate holes;

removing the protective oxide layer, the pad oxide layer, and the etch stopping layer;

forming a gate oxide layer in both the memory cell region and the peripheral region, the gate oxide layer penetrating the plurality of recessed gate holes in the cell region;

forming a gate layer on the gate oxide layer, including within the plurality of recessed gate holes; and

simultaneously forming recessed gates for the plurality of memory cells and planar gates for the plurality of transistors in the peripheral region.

21. The method of claim 20, further comprising implanting a substrate isolation in the memory cell region.

22. The method of claim 20, further comprising performing a threshold implantation in the plurality of memory cells.

23. The method of claim 20, further comprising performing a source/drain implantation in the plurality of memory cells;

24. The method of claim 20, further comprising simultaneously forming spacers on the plurality of memory cells and the plurality of transistors in the peripheral region.

25. The method of claim 24, further comprising, after forming spacers on the plurality of memory cells, forming a cobalt-silicon layer on the transistors in the peripheral region.

26. The method of claim 24, wherein forming a cobalt-silicon layer comprises:

maintaining a covering layer on the cell region;

selectively growing an epitaxial structure on plurality of transistors in the peripheral region; and

forming the cobalt-silicon layer on the epitaxial structure.

27. A memory device comprising:

a substrate divided into a cell region and a peripheral region;

a plurality of memory cells formed in the cell region, the plurality of memory cells each having a recessed gate structure; and

a plurality of transistors in the peripheral region, the plurality of transistors each having a recessed gate structure.

28. The memory device of claim 27 wherein gates of the memory cells in the cell region and gates of the cells in the peripheral region are formed simultaneously.